\*\*\* Running vivado

with args -log decoder.vdi -applog -m64 -product Vivado -messageDb vivado.pb -mode batch -source decoder.tcl -notrace

\*\*\*\*\*\* Vivado v2017.2 (64-bit)

\*\*\*\* SW Build 1909853 on Thu Jun 15 18:39:09 MDT 2017

\*\*\*\* IP Build 1909766 on Thu Jun 15 19:58:00 MDT 2017

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source decoder.tcl -notrace

Design is defaulting to srcset: sources\_1

Design is defaulting to constrset: constrs\_1

INFO: [Netlist 29-17] Analyzing 2 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-479] Netlist was created with Vivado 2017.2

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Project 1-570] Preparing netlist for logic optimization

Parsing XDC File [T:/decoder/decoder.srcs/constrs\_1/new/decoder\_property.xdc]

Finished Parsing XDC File [T:/decoder/decoder.srcs/constrs\_1/new/decoder\_property.xdc]

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Command: opt\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t-csg324'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t-csg324'

Running DRC as a precondition to command opt\_design

Starting DRC Task

Command: report\_drc (run\_mandatory\_drcs) for: opt\_checks

INFO: [DRC 23-27] Running DRC with 2 threads

report\_drc (run\_mandatory\_drcs) completed successfully

INFO: [Project 1-461] DRC finished with 0 Errors

INFO: [Project 1-462] Please refer to the DRC report (report\_drc) for more information.

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.065 . Memory (MB): peak = 496.383 ; gain = 4.293

INFO: [Timing 38-35] Done setting XDC timing constraints.

Starting Logic Optimization Task

Phase 1 Retarget

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Opt 31-49] Retargeted 0 cell(s).

Phase 1 Retarget | Checksum: 1dadfb04d

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.007 . Memory (MB): peak = 977.605 ; gain = 0.000

INFO: [Opt 31-389] Phase Retarget created 0 cells and removed 0 cells

Phase 2 Constant propagation

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Phase 2 Constant propagation | Checksum: 1dadfb04d

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.008 . Memory (MB): peak = 977.605 ; gain = 0.000

INFO: [Opt 31-389] Phase Constant propagation created 0 cells and removed 0 cells

Phase 3 Sweep

Phase 3 Sweep | Checksum: 1dadfb04d

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.009 . Memory (MB): peak = 977.605 ; gain = 0.000

INFO: [Opt 31-389] Phase Sweep created 0 cells and removed 0 cells

Phase 4 BUFG optimization

Phase 4 BUFG optimization | Checksum: 1dadfb04d

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.010 . Memory (MB): peak = 977.605 ; gain = 0.000

INFO: [Opt 31-389] Phase BUFG optimization created 0 cells and removed 0 cells

Phase 5 Shift Register Optimization

Phase 5 Shift Register Optimization | Checksum: 1dadfb04d

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.010 . Memory (MB): peak = 977.605 ; gain = 0.000

INFO: [Opt 31-389] Phase Shift Register Optimization created 0 cells and removed 0 cells

Starting Connectivity Check Task

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 977.605 ; gain = 0.000

Ending Logic Optimization Task | Checksum: 1dadfb04d

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.011 . Memory (MB): peak = 977.605 ; gain = 0.000

Starting Power Optimization Task

INFO: [Pwropt 34-132] Skipping clock gating for clocks with a period < 2.00 ns.

Ending Power Optimization Task | Checksum: 1dadfb04d

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.005 . Memory (MB): peak = 977.605 ; gain = 0.000

21 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.

opt\_design completed successfully

opt\_design: Time (s): cpu = 00:00:10 ; elapsed = 00:00:09 . Memory (MB): peak = 977.605 ; gain = 485.516

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.033 . Memory (MB): peak = 977.605 ; gain = 0.000

INFO: [Common 17-1381] The checkpoint 'T:/decoder/decoder.runs/impl\_1/decoder\_opt.dcp' has been generated.

Command: report\_drc -file decoder\_drc\_opted.rpt

INFO: [DRC 23-27] Running DRC with 2 threads

INFO: [Coretcl 2-168] The results of DRC are in file T:/decoder/decoder.runs/impl\_1/decoder\_drc\_opted.rpt.

report\_drc completed successfully

INFO: [Chipscope 16-241] No debug cores found in the current design.

Before running the implement\_debug\_core command, either use the Set Up Debug wizard (GUI mode)

or use the create\_debug\_core and connect\_debug\_core Tcl commands to insert debug cores into the design.

Command: place\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t-csg324'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t-csg324'

Command: report\_drc (run\_mandatory\_drcs) for: incr\_eco\_checks

INFO: [DRC 23-27] Running DRC with 2 threads

report\_drc (run\_mandatory\_drcs) completed successfully

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Running DRC as a precondition to command place\_design

Command: report\_drc (run\_mandatory\_drcs) for: placer\_checks

INFO: [DRC 23-27] Running DRC with 2 threads

report\_drc (run\_mandatory\_drcs) completed successfully

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Placer Task

INFO: [Place 30-611] Multithreading enabled for place\_design using a maximum of 2 CPUs

Phase 1 Placer Initialization

Phase 1.1 Placer Initialization Netlist Sorting

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00 . Memory (MB): peak = 977.605 ; gain = 0.000

Phase 1.1 Placer Initialization Netlist Sorting | Checksum: 13332b5e5

Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.002 . Memory (MB): peak = 977.605 ; gain = 0.000

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.001 . Memory (MB): peak = 977.605 ; gain = 0.000

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device

INFO: [Timing 38-35] Done setting XDC timing constraints.

Phase 1.2 IO Placement/ Clock Placement/ Build Placer Device | Checksum: 13332b5e5

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.511 . Memory (MB): peak = 977.605 ; gain = 0.000

Phase 1.3 Build Placer Netlist Model

Phase 1.3 Build Placer Netlist Model | Checksum: 1dddff8bb

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.516 . Memory (MB): peak = 977.605 ; gain = 0.000

Phase 1.4 Constrain Clocks/Macros

Phase 1.4 Constrain Clocks/Macros | Checksum: 1dddff8bb

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.517 . Memory (MB): peak = 977.605 ; gain = 0.000

Phase 1 Placer Initialization | Checksum: 1dddff8bb

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.518 . Memory (MB): peak = 977.605 ; gain = 0.000

Phase 2 Global Placement

WARNING: [Place 46-30] place\_design is not in timing mode. Skip physical synthesis in placer

Phase 2 Global Placement | Checksum: 18d871438

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.689 . Memory (MB): peak = 977.605 ; gain = 0.000

Phase 3 Detail Placement

Phase 3.1 Commit Multi Column Macros

Phase 3.1 Commit Multi Column Macros | Checksum: 18d871438

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.691 . Memory (MB): peak = 977.605 ; gain = 0.000

Phase 3.2 Commit Most Macros & LUTRAMs

Phase 3.2 Commit Most Macros & LUTRAMs | Checksum: 17154ccd7

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.700 . Memory (MB): peak = 977.605 ; gain = 0.000

Phase 3.3 Area Swap Optimization

Phase 3.3 Area Swap Optimization | Checksum: 204dda132

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.711 . Memory (MB): peak = 977.605 ; gain = 0.000

Phase 3.4 Pipeline Register Optimization

Phase 3.4 Pipeline Register Optimization | Checksum: 204dda132

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.711 . Memory (MB): peak = 977.605 ; gain = 0.000

Phase 3.5 Small Shape Detail Placement

Phase 3.5 Small Shape Detail Placement | Checksum: 25734fa0e

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.839 . Memory (MB): peak = 977.605 ; gain = 0.000

Phase 3.6 Re-assign LUT pins

Phase 3.6 Re-assign LUT pins | Checksum: 25734fa0e

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.839 . Memory (MB): peak = 977.605 ; gain = 0.000

Phase 3.7 Pipeline Register Optimization

Phase 3.7 Pipeline Register Optimization | Checksum: 25734fa0e

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.840 . Memory (MB): peak = 977.605 ; gain = 0.000

Phase 3 Detail Placement | Checksum: 25734fa0e

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.840 . Memory (MB): peak = 977.605 ; gain = 0.000

Phase 4 Post Placement Optimization and Clean-Up

Phase 4.1 Post Commit Optimization

Phase 4.1 Post Commit Optimization | Checksum: 25734fa0e

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.842 . Memory (MB): peak = 977.605 ; gain = 0.000

Phase 4.2 Post Placement Cleanup

Phase 4.2 Post Placement Cleanup | Checksum: 25734fa0e

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.844 . Memory (MB): peak = 977.605 ; gain = 0.000

Phase 4.3 Placer Reporting

Phase 4.3 Placer Reporting | Checksum: 25734fa0e

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.844 . Memory (MB): peak = 977.605 ; gain = 0.000

Phase 4.4 Final Placement Cleanup

Phase 4.4 Final Placement Cleanup | Checksum: 25734fa0e

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.844 . Memory (MB): peak = 977.605 ; gain = 0.000

Phase 4 Post Placement Optimization and Clean-Up | Checksum: 25734fa0e

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.845 . Memory (MB): peak = 977.605 ; gain = 0.000

Ending Placer Task | Checksum: 1a017747a

Time (s): cpu = 00:00:01 ; elapsed = 00:00:00.851 . Memory (MB): peak = 977.605 ; gain = 0.000

34 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

place\_design completed successfully

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.038 . Memory (MB): peak = 977.605 ; gain = 0.000

INFO: [Common 17-1381] The checkpoint 'T:/decoder/decoder.runs/impl\_1/decoder\_placed.dcp' has been generated.

report\_io: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.029 . Memory (MB): peak = 977.605 ; gain = 0.000

report\_utilization: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.020 . Memory (MB): peak = 977.605 ; gain = 0.000

report\_control\_sets: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.003 . Memory (MB): peak = 977.605 ; gain = 0.000

Command: route\_design

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t-csg324'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t-csg324'

Running DRC as a precondition to command route\_design

Command: report\_drc (run\_mandatory\_drcs) for: router\_checks

INFO: [DRC 23-27] Running DRC with 2 threads

report\_drc (run\_mandatory\_drcs) completed successfully

INFO: [Vivado\_Tcl 4-198] DRC finished with 0 Errors

INFO: [Vivado\_Tcl 4-199] Please refer to the DRC report (report\_drc) for more information.

Starting Routing Task

INFO: [Route 35-254] Multithreading enabled for route\_design using a maximum of 2 CPUs

Checksum: PlaceDB: b5c679ba ConstDB: 0 ShapeSum: ea50fac0 RouteDB: 0

Phase 1 Build RT Design

Phase 1 Build RT Design | Checksum: f2bd27d5

Time (s): cpu = 00:00:21 ; elapsed = 00:00:19 . Memory (MB): peak = 1131.828 ; gain = 154.223

Phase 2 Router Initialization

INFO: [Route 35-64] No timing constraints were detected. The router will operate in resource-optimization mode.

Phase 2.1 Fix Topology Constraints

Phase 2.1 Fix Topology Constraints | Checksum: f2bd27d5

Time (s): cpu = 00:00:21 ; elapsed = 00:00:19 . Memory (MB): peak = 1134.984 ; gain = 157.379

Phase 2.2 Pre Route Cleanup

Phase 2.2 Pre Route Cleanup | Checksum: f2bd27d5

Time (s): cpu = 00:00:21 ; elapsed = 00:00:19 . Memory (MB): peak = 1134.984 ; gain = 157.379

Number of Nodes with overlaps = 0

Phase 2 Router Initialization | Checksum: b9bc3c6b

Time (s): cpu = 00:00:21 ; elapsed = 00:00:19 . Memory (MB): peak = 1137.613 ; gain = 160.008

Phase 3 Initial Routing

Phase 3 Initial Routing | Checksum: ac9ad0e7

Time (s): cpu = 00:00:21 ; elapsed = 00:00:19 . Memory (MB): peak = 1137.613 ; gain = 160.008

Phase 4 Rip-up And Reroute

Phase 4.1 Global Iteration 0

Number of Nodes with overlaps = 0

Phase 4.1 Global Iteration 0 | Checksum: f1cbcc0e

Time (s): cpu = 00:00:21 ; elapsed = 00:00:19 . Memory (MB): peak = 1137.613 ; gain = 160.008

Phase 4 Rip-up And Reroute | Checksum: f1cbcc0e

Time (s): cpu = 00:00:21 ; elapsed = 00:00:19 . Memory (MB): peak = 1137.613 ; gain = 160.008

Phase 5 Delay and Skew Optimization

Phase 5 Delay and Skew Optimization | Checksum: f1cbcc0e

Time (s): cpu = 00:00:21 ; elapsed = 00:00:19 . Memory (MB): peak = 1137.613 ; gain = 160.008

Phase 6 Post Hold Fix

Phase 6.1 Hold Fix Iter

Phase 6.1 Hold Fix Iter | Checksum: f1cbcc0e

Time (s): cpu = 00:00:21 ; elapsed = 00:00:19 . Memory (MB): peak = 1137.613 ; gain = 160.008

Phase 6 Post Hold Fix | Checksum: f1cbcc0e

Time (s): cpu = 00:00:21 ; elapsed = 00:00:19 . Memory (MB): peak = 1137.613 ; gain = 160.008

Phase 7 Route finalize

Router Utilization Summary

Global Vertical Routing Utilization = 0.00230665 %

Global Horizontal Routing Utilization = 0.000852515 %

Routable Net Status\*

\*Does not include unroutable nets such as driverless and loadless.

Run report\_route\_status for detailed report.

Number of Failed Nets = 0

Number of Unrouted Nets = 0

Number of Partially Routed Nets = 0

Number of Node Overlaps = 0

Congestion Report

North Dir 1x1 Area, Max Cong = 5.40541%, No Congested Regions.

South Dir 1x1 Area, Max Cong = 8.10811%, No Congested Regions.

East Dir 1x1 Area, Max Cong = 2.94118%, No Congested Regions.

West Dir 1x1 Area, Max Cong = 2.94118%, No Congested Regions.

Phase 7 Route finalize | Checksum: f1cbcc0e

Time (s): cpu = 00:00:21 ; elapsed = 00:00:19 . Memory (MB): peak = 1137.613 ; gain = 160.008

Phase 8 Verifying routed nets

Verification completed successfully

Phase 8 Verifying routed nets | Checksum: f1cbcc0e

Time (s): cpu = 00:00:21 ; elapsed = 00:00:19 . Memory (MB): peak = 1138.863 ; gain = 161.258

Phase 9 Depositing Routes

Phase 9 Depositing Routes | Checksum: f8d0921d

Time (s): cpu = 00:00:21 ; elapsed = 00:00:19 . Memory (MB): peak = 1138.863 ; gain = 161.258

INFO: [Route 35-16] Router Completed Successfully

Time (s): cpu = 00:00:21 ; elapsed = 00:00:19 . Memory (MB): peak = 1138.863 ; gain = 161.258

Routing Is Done.

42 Infos, 1 Warnings, 0 Critical Warnings and 0 Errors encountered.

route\_design completed successfully

route\_design: Time (s): cpu = 00:00:21 ; elapsed = 00:00:19 . Memory (MB): peak = 1138.863 ; gain = 161.258

Writing placer database...

Writing XDEF routing.

Writing XDEF routing logical nets.

Writing XDEF routing special nets.

Write XDEF Complete: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.033 . Memory (MB): peak = 1138.863 ; gain = 0.000

INFO: [Common 17-1381] The checkpoint 'T:/decoder/decoder.runs/impl\_1/decoder\_routed.dcp' has been generated.

Command: report\_drc -file decoder\_drc\_routed.rpt -pb decoder\_drc\_routed.pb -rpx decoder\_drc\_routed.rpx

INFO: [DRC 23-27] Running DRC with 2 threads

INFO: [Coretcl 2-168] The results of DRC are in file T:/decoder/decoder.runs/impl\_1/decoder\_drc\_routed.rpt.

report\_drc completed successfully

Command: report\_methodology -file decoder\_methodology\_drc\_routed.rpt -rpx decoder\_methodology\_drc\_routed.rpx

INFO: [Timing 38-35] Done setting XDC timing constraints.

INFO: [DRC 23-133] Running Methodology with 2 threads

INFO: [Coretcl 2-1520] The results of Report Methodology are in file T:/decoder/decoder.runs/impl\_1/decoder\_methodology\_drc\_routed.rpt.

report\_methodology completed successfully

Command: report\_power -file decoder\_power\_routed.rpt -pb decoder\_power\_summary\_routed.pb -rpx decoder\_power\_routed.rpx

WARNING: [Power 33-232] No user defined clocks were found in the design!

Resolution: Please specify clocks using create\_clock/create\_generated\_clock for sequential elements. For pure combinatorial circuits, please specify a virtual clock, otherwise the vectorless estimation might be inaccurate

INFO: [Timing 38-35] Done setting XDC timing constraints.

Running Vector-less Activity Propagation...

Finished Running Vector-less Activity Propagation

49 Infos, 2 Warnings, 0 Critical Warnings and 0 Errors encountered.

report\_power completed successfully

INFO: [Timing 38-91] UpdateTimingParams: Speed grade: -1, Delay Type: min\_max.

INFO: [Timing 38-191] Multithreading enabled for timing update using a maximum of 2 CPUs

WARNING: [Timing 38-313] There are no user specified timing constraints. Timing constraints are needed for proper timing analysis.

Command: write\_bitstream -force decoder.bit

Attempting to get a license for feature 'Implementation' and/or device 'xc7a100t-csg324'

INFO: [Common 17-349] Got license for feature 'Implementation' and/or device 'xc7a100t-csg324'

Running DRC as a precondition to command write\_bitstream

Command: report\_drc (run\_mandatory\_drcs) for: bitstream\_checks

INFO: [DRC 23-27] Running DRC with 2 threads

WARNING: [DRC CFGBVS-1] Missing CFGBVS and CONFIG\_VOLTAGE Design Properties: Neither the CFGBVS nor CONFIG\_VOLTAGE voltage property is set in the current\_design. Configuration bank voltage select (CFGBVS) must be set to VCCO or GND, and CONFIG\_VOLTAGE must be set to the correct configuration voltage, in order to determine the I/O voltage support for the pins in bank 0. It is suggested to specify these either using the 'Edit Device Properties' function in the GUI or directly in the XDC file using the following syntax:

set\_property CFGBVS value1 [current\_design]

#where value1 is either VCCO or GND

set\_property CONFIG\_VOLTAGE value2 [current\_design]

#where value2 is the voltage provided to configuration bank 0

Refer to the device configuration user guide for more information.

report\_drc (run\_mandatory\_drcs) completed successfully

INFO: [Vivado 12-3199] DRC finished with 0 Errors, 1 Warnings

INFO: [Vivado 12-3200] Please refer to the DRC report (report\_drc) for more information.

INFO: [Project 1-821] Please set project.enableDesignId to be 'true'.

INFO: [Designutils 20-2272] Running write\_bitstream with 2 threads.

Loading data files...

Loading site data...

Loading route data...

Processing options...

Creating bitmap...

Creating bitstream...

Writing bitstream ./decoder.bit...

INFO: [Vivado 12-1842] Bitgen Completed Successfully.

INFO: [Project 1-120] WebTalk data collection is mandatory when using a WebPACK part without a full Vivado license. To see the specific WebTalk data collected for your design, open the usage\_statistics\_webtalk.html or usage\_statistics\_webtalk.xml file in the implementation directory.

INFO: [Common 17-186] 'T:/decoder/decoder.runs/impl\_1/usage\_statistics\_webtalk.xml' has been successfully sent to Xilinx on Wed Jan 23 17:42:30 2019. For additional details about this file, please refer to the WebTalk help file at C:/Xilinx/Vivado/2017.2/doc/webtalk\_introduction.html.

60 Infos, 4 Warnings, 0 Critical Warnings and 0 Errors encountered.

write\_bitstream completed successfully

write\_bitstream: Time (s): cpu = 00:00:10 ; elapsed = 00:00:10 . Memory (MB): peak = 1527.102 ; gain = 365.633

INFO: [Common 17-206] Exiting Vivado at Wed Jan 23 17:42:31 2019...